SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-179132; filed on September 11, 2015; the entire contents of which are incorporated herein by reference.

FIELD

An embodiment described herein relates generally to a semiconductor device.

BACKGROUND

It is expected that silicon carbide (SiC) is used for a material for a next-generation semiconductor device. SiC has excellent physical properties in which a bandgap is three times, breakdown electric field strength is 10 times, and thermal conductivity is three times, compared to silicon (Si). By taking advantage of the characteristics, it is possible to realize a semiconductor device which has low loss and can perform an operation at a high temperature.

A device which uses SiC can operate at a high voltage by using a wider bandgap of the SiC. For this reason, for example, reliability of a gate insulating film to which a high electric field is applied becomes a problem.

An example of related art includes JP-A-2013-149837.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic sectional view illustrating a semiconductor device according to an embodiment.

FIG. 2 is a schematic sectional view illustrating the semiconductor device in the process of fabrication according to a fabrication method of the semiconductor device according to the embodiment.

FIG. 3 is a schematic sectional view illustrating the semiconductor device in the process of fabrication according to the fabrication method of the semiconductor device according to the embodiment.

FIG. 4 is a schematic sectional view illustrating the semiconductor device in the process of fabrication according to the fabrication method of the semiconductor device according to the embodiment.

FIG. 5 is a schematic sectional view illustrating the semiconductor device in the process of fabrication according to the fabrication method of the semiconductor device according to the embodiment.

FIG. 6 is a schematic sectional view illustrating the semiconductor device in the process of fabrication according to the fabrication method of the semiconductor device according to the embodiment.

FIG. 7 is a schematic sectional view illustrating a semiconductor device according to a comparative form.

DETAILED DESCRIPTION

[0005]An exemplary embodiment provides a semiconductor device which can increase reliability of a gate insulating film.

[0006]In general, according to one embodiment, a semiconductor device includes a SiC layer including a first surface; a gate insulating film which is provided on the first surface; a gate insulating film which is provided on the gate electrode; a first SiC region of a first conductive type which is provided in the SiC layer and a portion of which is provided in the first surface; a second SiC region of a second conductive type which is provided in the first SiC region and a portion of which is provided in the first surface; a third SiC region of a first conductive type which is provided in the second SiC region, a portion of which is provided in the first surface, and has a first inclined angle between a boundary between the second SiC region and the third SiC region, and the first surface; and a fourth SiC region of a first conductive type which is provided in the third SiC region, a portion of which is provided in the first surface, in which impurity concentration of the first conductive type is higher than impurity concentration of the third SiC region, and which has a second inclined angle, that is smaller than the first inclined angle, between a boundary between the third SiC region and the fourth SiC region, and the first surface.

[0008]Hereinafter, an exemplary embodiment will be descried with reference to the drawings. In the following description, the same symbols or reference numerals will be attached to the same or similar members or the like, and description of the members or the like described once will be appropriately omitted.

[0009]In addition, in the following description, notation of n++, n+, n and n-, and p++, p+, p and p- represents relative levels of impurity concentrations of each conductive type. That is, it represents that n++-type impurity concentration is relatively higher than n+-type impurity concentration, n+-type impurity concentration is relatively higher than n-type impurity concentration, and n--type impurity concentration is relatively lower than n-type impurity concentration. In addition, it represents that p++-type impurity concentration is relatively higher than p+-type impurity concentration, p+-type impurity concentration is relatively higher than p-type impurity concentration, and p--type impurity concentration is relatively lower than p-type impurity concentration. There is a case in which n+ and n- are simply described as an n-type, and p+ and p- are simply described as a p-type.

[0010]A semiconductor device according to the embodiment includes a SiC layer including a first surface; a gate insulating film which is provided on the first surface; a gate electrode which is provided on the gate insulating film; a first SiC region of a first conductive type which is provided in the SiC layer and a portion of which is provided in the first surface; a second SiC region of a second conductive type which is provided in the first SiC region and a portion of which is provided in the first surface; a third SiC region of a first conductive type which is provided in the second SiC region, a portion of which is provided in the first surface, and has a first inclined angle between a boundary between the second SiC region and the third SiC region, and the first surface; and a fourth SiC region of a first conductive type which is provided in the third SiC region, a portion of which is provided in the first surface, in which impurity concentration of the first conductive type is higher than impurity concentration of the third SiC region, and which has a second inclined angle, that is smaller than the first inclined angle, between a boundary between the third SiC region and the fourth SiC region, and the first surface.

[0011]FIG. 1 is a schematic sectional view illustrating a configuration of a metal oxide semiconductor field effect transistor (MOSFET) which is a semiconductor device according to the embodiment. The MOSFET 100 includes a well region and a source region which are formed by, for example, ion injection, and is a double implantation MOSFET (DIMOSFET). The MOSFET 100 is a vertical n-channel MOSFET which uses electrons as carriers.

[0012]The MOSFET 100 includes a SiC substrate 10, a SiC layer 12, a source electrode (first electrode) 14, a drain electrode (second electrode) 16, a gate insulating film 18, a gate electrode 20, and an interlayer insulating film 22. The SiC layer 12 includes a drift region (first SiC region) 24, a well region (second SiC region) 26, a source region (third SiC region) 30, a source contact region (fourth SiC region) 32, and a well contact region 34.

[0013]The SiC substrate 10 is a SiC of single crystal. The SiC substrate 10 is, for example, 4H-SiC. A case in which an upper surface of the SiC substrate 10 is a surface inclined to an angle greater than or equal to zero degrees and smaller than or equal to eight degrees with respect to a (0001) surface, and a lower surface is a surface inclined to an angle greater than or equal to zero degrees and smaller than or equal to eight degrees with respect to (000-1) surface will be described as an example. The (0001) surface is symmetric with a silicon surface. The (000-1) surface is symmetric with a carbon surface.

[0014]The SiC substrate 10 is a drain region of the MOSFET 100. The SiC substrate 10 is an n-type SiC. The SiC substrate 10 contains, for example, nitride (N) as n-type impurity. The n-type impurity concentration of the SiC substrate 10 is, for example, higher than or equal to 1´1018 cm-3 and lower than or equal to 1´1021 cm-3.

[0015]It is preferable that the n-type impurity concentration of a lower surface of the SiC substrate 10 is higher than or equal to 1´1019 cm-3, and it is more preferable that the n-type impurity concentration of a lower surface of the SiC substrate 10 is higher than or equal to 1´1020 cm-3, from a viewpoint in which a contact resistance between the drain electrode 16 and the SiC substrate 10 is reduced.

[0016]The SiC layer 12 is provided on the SiC substrate 10. The SiC layer 12 is a single crystal SiC which is formed on the SiC substrate 10 by epitaxial growth.

[0017]The SiC layer 12 includes a first surface (hereinafter, will also be simply described as a surface). The first surface is, for example, a surface inclined to an angle greater than or equal to zero degrees and smaller than or equal to eight degrees with respect to a (0001) surface.

[0018]The drift region 24 is provided in the SiC layer 12. At least a portion of the drift region 24 is provided on a surface of the SiC layer 12. The drift region 24 is provided on the SiC substrate 10.

[0019]The drift region 24 is an n-type SiC. The drift region 24 contains, for example, nitride (N) as an n-type impurity. The n-type impurity concentration of the drift region 24 is higher than or equal to 5´1015 cm-3 and lower than or equal to 2´1016 cm-3. A thickness of the drift region 24 is, for example, greater than or equal to 5 mm and smaller than or equal to 150 mm.

[0020]The well region 26 is provided in the SiC layer 12. The well region 26 is provided in the drift region 24. At least a portion of the well region 26 is provided on a surface of the SiC layer 12.

[0021]The well region 26 is a p-type SiC. The well region 26 functions as a channel area of the MOSFET 100.

[0022]The well region 26 contains, for example, aluminum (Al) as a p-type impurity. The p-type impurity concentration of the well region 26 is, for example, higher than or equal to 5´1015 cm-3 and lower than or equal to 1´1018 cm-3. A depth of the well region 26 is, for example, greater than or equal to 0.4 mm and smaller than or equal to 0.8 mm.

[0023]The source region 30 is provided in the SiC layer 12. The source region 30 is provided in the well region 26. At least a portion of the source region 30 is provided on a surface of the SiC layer 12.

[0024]The source region 30 is an n+-type SiC. The source region 30 contains, for example, phosphorous (P) as an n-type impurity. The n-type impurity concentration of the source region 30 is, for example, higher than or equal to 1´1018 cm-3 and lower than 1´1020 cm-3. The n-type impurity concentration of the source region 30 is, for example, lower than or equal to 1´1019 cm-3. A depth the source region 30 is smaller than the depth of the well region 26, and is, for example, greater than or equal to 0.2 mm and smaller than or equal to 0.4 mm.

[0025]A boundary between the source region 30 and the well region 26 has a first inclined angle (q1) between the boundary and a surface of the SiC layer 12. In other words, an angle between the boundary between the source region 30 and the well region 26, and the surface of the SiC layer is the first inclined angle (q1). The first inclined angle (q1) is, for example, greater than or equal to 80 degrees and smaller than or equal to 90 degrees.

[0026]The source contact region 32 is provided in the SiC layer 12. The source contact region 32 is provided in the source region 30. At least a portion of the source contact region 32 is provided on the surface of the SiC layer 12.

[0027]The source contact region 32 is an n++-type SiC. The source contact region 32 contains, for example, phosphorous (P) as n-type impurity. The n-type impurity concentration of the source contact region 32 is higher than n-type impurity of the source region 30. The n-type impurity concentration of the source contact region 32 is, for example, higher than or equal to 1´1019 cm-3 and lower than 1´1022 cm-3. The n-type impurity concentration of the source contact region 32 is, for example, lower than or equal to 1´1020 cm-3. A depth the source contact region 32 is smaller than the depth of the source region 30, and is, for example, greater than or equal to 0.05 mm and smaller than or equal to 0.2 mm.

[0028]A boundary between the source contact region 32 and the source region 30 has a second inclined angle (q2) between the boundary and the surface of the SiC layer 12. In other words, an angle between the boundary between the source contact region 32 and the source region 30, and the surface of the SiC layer is the second inclined angle (q2).

[0029]The second inclined angle (q2) is smaller than the first inclined angle (q1). The second inclined angle (q2) is, for example, greater than or equal to 45 degrees and smaller than 80 degrees. The second inclined angle (q2) is, for example, smaller than or equal to 60 degrees.

[0030]The gate electrode 20 and the source contact region 32 are separated from each other in a direction parallel to the surface of the SiC layer 12. A distance (“d” of FIG. 1) between the gate electrode 20 and the source contact region 32 is, for example, more than or equal to 0.1 mm and less than or equal to 1.0 mm.

[0031]The well contact region 34 is provided in the SiC layer 12. The well contact region 34 is provided in the well region 26. The well contact region 34 is provided so as to be interposed between the source regions 30.

[0032]The well contact region 34 is a p+-type SiC. The well contact region 34 contains, for example, aluminum (Al) as p-type impurity. Impurity concentration of the p-type impurity of the well contact region 34 is, for example, higher than or equal to 1´1018 cm-3 and lower than or equal to 1´1022 cm-3.

[0033]A depth of the well contact region 34 is smaller than a depth of the well region 26, and is, for example, greater than or equal to 0.2 mm and smaller than or equal to 0.4 mm.

[0034]The gate insulating film 18 is provided on the surface of the SiC layer 12. The gate insulating film 18 is provided on the drift region 24, the well region 26, and the source region 30. The gate insulating film 18 is, for example, a silicon oxide film. For example, a high-k insulating film (high dielectric constant insulating film) can be applied to the gate insulating film 18.

[0035]The gate electrode 20 is provided on the gate insulating film 18. The gate insulating film 18 is a conductive layer. The gate electrode 20 is, for example, polycrystalline silicon which contains conductive impurity.

[0036]The interlayer insulating film 22 is provided on the gate electrode 20. The interlayer insulating film 22 is, for example, a silicon oxide film.

[0037]The well region 26 which is interposed between the source region 30 under the gate electrode 20 and the drift region 24 functions as a channel region of the MOSFET 100.

[0038]The source electrode 14 is provided on the surface of the SiC layer 12. The source electrode 14 is electrically coupled to the source contact region 32 and the well contact region 34. The source electrode 14 comes into contact with the source contact region 32 and the well contact region 34. The source electrode 14 has a function of supplying a potential to the well region 26.

[0039]The source electrode 14 is, for example, a metal. A metal which forms the SiC layer 12 is, for example, a laminated structure of titanium (Ti) and aluminum (Al). It doesn’t matter that the source electrode 14 contains metal silicide or metal carbide which comes into contact with the SiC layer 12.

[0040]The drain electrode 16 is provided on a rear surface of the SiC substrate 10. The drain electrode 16 is electrically coupled to the SiC substrate 10.

[0041]The drain electrode 16 is a metal such as, titanium (Ti), nickel (Ni), gold (Au) or silver (Ag), or metal silicide.

[0042]The first inclined angle (q1) and the second inclined angle (q2) can be measured by using a scanning capacitance microscopy (SCM) method. For example, the first inclined angle (q1) is set by drawing a tangent line of a boundary between the source region 30 and the well region 26, near a point at which the boundary between the source region 30 and the well region 26 intersects the first surface, from concentration profile which is observed by the SCM method, and then calculating an angle between the tangent line and the first surface. In addition, for example, the second inclined angle (q2) is set by drawing a tangent line of a boundary between the source contact region 32 and the well region 26, near a point at which the boundary between the source contact region 32 and the source region 30 intersects the first surface, from the concentration profile which is observed by the SCM method, and then, calculating an angle between the tangent line and the first surface.

[0043]Impurity concentration of the impurity region can be measured by using a secondary ion mass spectrometry (SIMS) method.

[0044]Next, a fabrication method of the semiconductor device according to the embodiment will be described. FIGS. 2 to 6 are schematic sectional views illustrating the semiconductor device in the process of fabrication according to the fabrication method of the semiconductor device according to the embodiment.

[0045]The SiC layer 12 is formed on the SiC substrate 10 by epitaxial growth. The SiC layer 12 includes a first surface (hereinafter, will also be simply described as a surface).

[0046]Subsequently, a first mask member 50 is formed on the surface of the SiC layer 12. The first mask member 50 is a silicon oxide film which is formed by using, for example, a chemical vapor deposition (CVD) method.

[0047]Subsequently, ion injection of aluminum (Al), which is a p-type impurity, into the drift region 24 is performed by using the first mask member 50 (FIG. 2). The well region 26 is formed by the ion injection.

[0048]Subsequently, a second mask member 52 is laminated on the first mask member 50 and the surface of the SiC layer 12 (FIG. 3). The second mask member 52 is a silicon oxide film which is formed by using, for example, a chemical vapor deposition (CVD) method.

[0049]Subsequently, the second mask member 52 is etched by using a reactive ion etching (RIE) method, and processing is performed such that the second mask member 52 remains on both sides of the first mask member 50. Thereafter, ion injection of phosphorous (P) which is n-type impurity into the well region 26 is performed by using the first mask member 50 and the second mask member 52 as masks (FIG. 4). The source region 30 is formed by ion injection.

[0050]For example, both side surfaces of the second mask member 52 have the first inclined angle (q1). In this case, the shape of the second mask member 52 is reflected, and an angle between a boundary between the source region 30 and the well region 26, and the surface of the SiC substrate 10 becomes the first inclined angle (q1).

[0051]Subsequently, a third mask member 54 is laminated on the first mask member 50, the second mask member 52, and the surface of the SiC layer 12 (FIG. 5). The third mask member 54 is a silicon oxide film which is formed by using, for example, the CVD method.

[0052]Subsequently, the third mask member 54 is etched by using the RIE method, and processing is performed such that the third mask member 54 remains on both sides of the second mask member 52. Thereafter, ion injection of phosphorous (P) which is n-type impurity into the source region 30 is performed by using the first mask member 50, the second mask member 52, and the third mask member 54 as masks (FIG. 6). The source contact region 32 is formed by ion injection.

[0053]When the third mask member 54 is etched, etching conditions are controlled such that both side surfaces of the third mask member 54 has the second inclined angle (q2) smaller than the first inclined angle (q1). In this case, the shape of the third mask member 54 is reflected, and an angle between a boundary between the source contact region 32 and the source region 30, and the surface of the SiC layer 12 becomes the second inclined angle (q2).

[0054]Thereafter, the p-type well contact region 34 is formed in the SiC layer 12 by the known process.

[0055]Subsequently, the first mask member 50, the second mask member 52, and the third mask member 54 are removed by wet etching. Subsequently, annealing for activating the p-type impurity and n-type impurity is performed. For example, activation annealing is performed under temperature which is higher than or equal to 1700°C and lower than or equal to 1900°C in inert gas atmosphere.

[0056]Diffusion speed of the p-type impurity and the n-type impurity in SiC is much slower than diffusion speed of the p-type impurity and the n-type impurity in silicon (Si). Hence, profile of the p-type impurity and the n-type impurity shortly after the ion injection according to the embodiment is maintained without a great change even after the activation annealing. Hence, the first inclined angle (q1) and the second inclined angle (q2) are also maintained without a great change.

[0057]Subsequently, the gate insulating film 18 is formed on the surface of the SiC substrate 10. The gate insulating film 18 is a silicon oxide film which is formed by using, for example, the CVD method.

[0058]Subsequently, the gate electrode 20 is formed on the gate insulating film 18. The gate electrode 20 is, for example, polycrystalline silicon which contains conductive impurity.

[0059]Subsequently, the interlayer insulating film 22 is formed on the gate insulating film 18 and the gate electrode 20. The interlayer insulating film 22 is formed by laminating a silicon oxide film by using, for example, the CVD method and thereafter, patterning the silicon oxide film.

[0060]Subsequently, the source electrode 14 is formed on the source contact region 32 and the well contact region 34. The source electrode 14 is formed by sputtering, for example, titanium (Ti) and aluminum (Al).

[0061]Subsequently, the drain electrode 16 is formed on a rear surface of the SiC substrate 10. The drain electrode 16 is formed by sputtering, for example, Ti, Ni, Au, Ag, or the like. In addition, there is a case in which metal silicide is formed by performing thermal processing such as, sinter or rapid thermal annealing (RTA).

[0062]By the aforementioned fabrication method, the MOSFET 100 illustrated in FIG. 1 is formed.

[0063]Hereinafter, actions and effects of the semiconductor device according to the embodiment will be described.

[0064]FIG. 7 is a schematic sectional view illustrating a configuration of a MOSFET 900 which is a semiconductor device according to a comparative form.

[0065]The MOSFET 900 according to the comparative form is different from the MOSFET 100 according to the embodiment in that the first inclined angle (q1) is the same as the second inclined angle (q2). In addition, the MOSFET 900 the first inclined angle (q1) and the second inclined angle (q2) are 90 degrees.

[0066]In the MOSFET 900, a contact resistance between the source region 30 and the source electrode 14 decreases, and thus the source contact region 32 whose n-type impurity concentration is higher than n-type impurity concentration of the source region 30 is provided. If n-type impurity concentration of the entire source region 30 increases, a problem occurs in which a junction leakage current causing crystal defect increases. The crystal defect is caused by damage at the time of ion injection for forming an n-type region with a high concentration. For this reason, the MOSFET 900 employs a source structure in which the source contact region 32 with high concentration of n-type impurity is surrounded by the source region 30 with a low concentration of n-type impurity.

[0067]When the MOSFET 900 is turned off, a high voltage is applied between the gate electrode 20, the source region 30, and the source contact region 32. For this reason, a high electric field is applied to the gate insulating film 18 between the gate electrode 20, the source region 30, and the source contact region 32, time dependent dielectric breakdown of the gate insulating film 18 becomes a problem. Hence, there is a possibility that reliability of the MOSFET 900 decreases.

[0068]An electric field which is applied to the gate insulating film 18 increases, particularly on a corner portion of the gate electrode 20. The electric field which is applied to the gate insulating film 18 from the corner portion of the gate electrode 20 depends upon the impurity concentration of the SiC layer 12 near a lower portion of the corner portion of the gate electrode 20. If the impurity concentration of the SiC layer 12 near the lower portion of the corner portion of the gate electrode 20 is increased, an electric field in the gate insulating film 18 near the corner portion of the gate electrode 20 increases.

[0069]Particularly, if the source contact region 32 with a high impurity concentration becomes close to the gate electrode 20 or the source contact region 32 overlaps the gate electrode 20, in accordance with miniaturization of the MOSFET 900, the electric field in the gate insulating film 18 on the corner portion of the gate electrode 20 becomes higher. Hence, there is a high possibility that reliability failure occurs due to time dependent dielectric breakdown of the gate insulating film 18.

[0070]In addition, it is considered that impurity trapped in the crystal defect in an impurity region moves into the gate insulating film 18 by an electric field, and is trapped in the impurity of the gate insulating film 18, as a factor other than the time dependent dielectric breakdown of the gate insulating film 18. The amount of crystal defect of the impurity region is proportional to the impurity concentration. Hence, if the impurity concentration of the SiC layer 12 near the lower portion of the corner portion of the gate electrode 20 is increased, there is a possibility that the amount of impurity trapped in the gate insulating film 18 is increased. For this reason, there is a high possibility that reliability failure occurs due to the time dependent dielectric breakdown of the gate insulating film 18.

[0071]In the MOSFET 100 according to the embodiment, the second inclined angle (q2) is smaller than the first inclined angle (q1), and thus, substantially, the impurity concentration of the SiC layer 12 near the lower portion of the corner portion of the gate electrode 20 is decreased. For this reason, the electric field in the gate insulating film 18 near the corner portion of the gate electrode 20 decreases, compared to the MOSFET 900. In addition, the amount of impurity trapped in the gate insulating film 18 is decreased, compared to the MOSFET 900. Hence, the reliability failure due to the time dependent dielectric breakdown of the gate insulating film 18 is prevented. Hence, reliability of the MOSFET 100 increases.

[0072]It is preferable that the second inclined angle (q2) is smaller than 80 degrees, and it is more preferable that the second inclined angle (q2) is smaller than or equal to 60 degrees, from a viewpoint in which the electric field in the gate insulating film 18 near the corner portion of the gate electrode 20 decreases. In addition, it is preferable that the second inclined angle (q2) is greater than or equal to 45 degrees, from a viewpoint in which formation of the second inclined angle (q2) is stabilized.

[0073]It is preferable that the first inclined angle (q1) is greater than or equal to 80 degrees and smaller than or equal to 90 degrees, from a viewpoint in which process variation of the first inclined angle (q1) is prevented and a channel length of the MOSFET 100, that is, a distance between the drift region 24 and the source region 30 which are immediately below the gate insulating film 18 is stabilized.

[0074]It is preferable that the gate electrode 20 and the source contact region 32 are separated from each other in a direction parallel to the surface of the SiC layer 12, from a viewpoint in which impurity concentration of the SiC layer 12 near the lower portion of the corner portion of the gate electrode 20 is decreased.

[0075]It is preferable that the n-type impurity concentration of the source contact region 32 is higher than or equal to 1´1019 cm-3, and it is more preferable that the n-type impurity concentration of the source contact region 32 is higher than or equal to 1´1020 cm-3, from a viewpoint in which the contact resistance between the source electrode 14 and the source contact region 32 decreases.

[0076]It is preferable that the n-type impurity concentration of the source region 30 is lower than or equal to 5´1019 cm-3, and it is more preferable that the n-type impurity concentration of the source region 30 is lower than or equal to 1´1019 cm-3, from a viewpoint in which the crystal defect of the source region 30 decreases and a junction leakage current decreases.

[0077]As such, according to the MOSFET 100 according to the embodiment, reliability of a gate insulating film is increased.

[0078]In the embodiment, a case in which 4H-SiC is used as a SiC substrate is used as an example, but other crystal types such as 3C-SiC or 6H-SiC can also be used.

[0079]In the embodiment, an example in which nitride (N) and phosphorous (P) are used as n-type impurity is described, but arsenic (As), antimony (Sb) or the like can also be applied. In addition, an example in which aluminum (Al) is used as p-type impurity is described, but boron (B) can also be used.

[0080]In addition, in the embodiment, an example in which a vertical MOSFET is used as a semiconductor device, but if a semiconductor device includes a transistor having a metal insulator semiconductor (MIS) structure, the semiconductor device is not limited to a vertical MOSFET, and can apply an exemplary embodiment. For example, an exemplary embodiment can also be applied to a horizontal MOSFET. In addition, for example, an exemplary embodiment can also be applied to a vertical insulated gate bipolar transistor (IGBT).

[0081]In addition, in the embodiment, an example in which an n-type is used as the first conductive type and a p-type is used as the second conductive type is described, but it is also possible to use a p-type as the first conductive type and an n-type as the second conductive type. In this case, a transistor becomes a p-channel transistor which uses holes as carriers.

[0082]While a certain embodiment has been described, this embodiment has been presented by way of example only, and is not intended to limit the scope of the invention. Indeed, the novel embodiment described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiment described herein may be made without departing from the spirit of the invention. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the invention.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a SiC layer including a first surface;

a gate insulating film which is provided on the first surface;

a gate electrode which is provided on the gate insulating film;

a first SiC region of a first conductive type which is provided in the SiC layer and a portion of which is provided in the first surface;

a second SiC region of a second conductive type which is provided in the first SiC region and a portion of which is provided in the first surface;

a third SiC region of a first conductive type which is provided in the second SiC region, a portion of which is provided in the first surface, and has a first inclined angle between a boundary between the second SiC region and the third SiC region, and the first surface; and

a fourth SiC region of a first conductive type which is provided in the third SiC region, a portion of which is provided in the first surface, in which impurity concentration of the first conductive type is higher than impurity concentration of the third SiC region, and which has a second inclined angle, that is smaller than the first inclined angle, between a boundary between the third SiC region and the fourth SiC region, and the first surface.

2. The device according to Claim 1, wherein the gate insulating film is provided on the first SiC region, the second SiC region, and the third SiC region.

3. The device according to Claim 1 or 2, wherein the second inclined angle is greater than or equal to 45 degrees and smaller than 80 degrees.

4. The device according to any one of Claims 1 to 3, wherein the first inclined angle is greater than or equal to 80 degrees.

5. The device according to any one of Claims 1 to 4, wherein the gate electrode and the fourth SiC region are separated from each other in a direction parallel to the first surface.

6. The device according to any one of Claims 1 to 5, wherein impurity concentration of the first conductive type of the fourth SiC region is higher than or equal to 1´1020 cm-3.

7. The device according to any one of Claims 1 to 6, wherein impurity concentration of the first conductive type of the third SiC region is lower than or equal to 1´1019 cm-3.

8. The device according to any one of Claims 1 to 7, wherein the gate insulating film is a silicon oxide film.

9. The device according to any one of Claims 1 to 8, further comprising:

a first electrode which is provided on the fourth SiC region.

10. The device according to Claim 9, further comprising:

a second electrode which is provided so as to interpose the SiC layer between the first electrode and the second electrode.

ABSTRACT

According to one embodiment, a semiconductor device includes a SiC layer including a first surface; a gate insulating film which is provided on the first surface; a gate electrode which is provided on the gate insulating film; a first SiC region of a first conductive type which is provided in the SiC layer and a portion of which is provided in the first surface; a second SiC region of a second conductive type which is provided in the first SiC region and a portion of which is provided in the first surface; a third SiC region of a first conductive type which is provided in the second SiC region, a portion of which is provided in the first surface, and has a first inclined angle between a boundary between the second SiC region and the third SiC region, and the first surface; and a fourth SiC region of a first conductive type which is provided in the third SiC region, a portion of which is provided in the first surface, in which impurity concentration of the first conductive type is higher than impurity concentration of the third SiC region, and which has a second inclined angle, that is smaller than the first inclined angle, between a boundary between the third SiC region and the fourth SiC region, and the first surface.

DRAWING

FIG. 1

FIRST SURFACE

FIG. 2

FIRST SURFACE

FIG. 3

FIRST SURFACE

FIG. 4

FIRST SURFACE

FIG. 5

FIRST SURFACE

FIG. 6

FIRST SURFACE

FIG. 7

FIRST SURFACE